Modeling and Simulation of Switching Noise Including Power/Ground Plane Resonance for High Speed GaAs FET Logic (FL) Circuits

Jyh–Ming Jong and Vijai K. Tripathi
Department of Electrical and Computer Engineering
Oregon State University
Corvallis, OR 97331

ABSTRACT

Equivalent circuit models of power/ground plane structures in high speed/frequency electronic packages used for switching noise and ground bounce simulation are presented. As an example, the effect of package resonance on the switching noise due to edge and clock rates of the GaAs FET logic (FL) inverter is reported for a typical MLC package.

INTRODUCTION

The switching noise, caused by transient current flowing into power/ground distribution systems, is referred as ground bounce or Delta–I noise. With the advancement in high speed devices, a considerable amount of work has been done in recent years on the switching noise and ground bounce due to nonideal power/ground planes in high speed digital and RF circuits [1–4]. In addition to the electromagnetic computational methods for modeling the power/ground systems in electronic packages, time and frequency domain measurement techniques must be formulated to validate these models and to develop new measurement based circuit models which can be used during the design cycles in standard CAD tools [5–8]. In this paper, a typical parallel plane power and ground system in a MLC package as shown in Figure 1 is characterized by the nonuniform transmission line model (NTL) which is then used to study switching noise and ground bounce in high speed circuits. The NTL model is in a form of the cascaded piecewise impedance line sections where the corresponding characteristic impedances of the lines are synthesized from the time domain reflection measurement. An alternative lumped element equivalent network for circuit modeling of power/ground plane structures from time domain measurements is also presented.

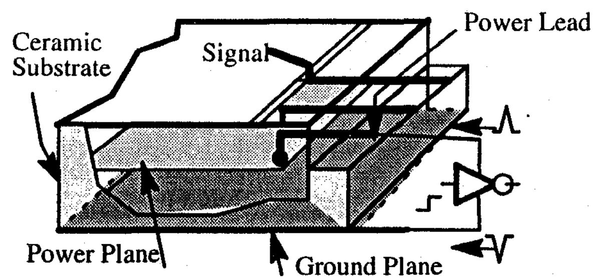


Figure 1, A schematic MLC package.

CIRCUIT MODELING OF PARALLEL POWER/GROUND PLANE STRUCTURES

For a simple semi–infinite parallel conducting plane structure as shown in Figure 2, the characteristic impedance profile of the NTL model can be obtained by using radial transmission line analysis. The frequency dependent nonuniform characteristic impedance corresponding to this model is found to be [5]

$$Z_o(r) = \frac{h}{\alpha r}\sqrt{\frac{\mu}{\epsilon}}\,\frac{G_0(kr)}{G_1(kr)}$$

which can be approximated by

$$Z_o(r) = \sqrt{\frac{\mu}{\epsilon}}\,\frac{h}{\alpha r}$$

at high frequencies (i.e., for $kr >> 1$). Here, α is the sector angle shown in Figure 2. This nonuniform impedance profile has been validated by TDR measurements as reported in [5]. As an example, the measured time domain reflection voltages together with the measured characteristic impedance profiles for three cases of 90 mil FR–4 substrate right angle sector, a half plane and 270^0 sector are shown in Figure 3. It is obvious that the measured nonuniform impedance profiles depend on the degree α .

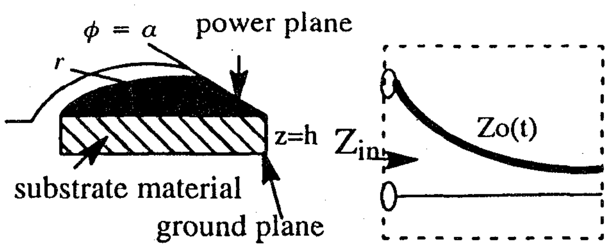


Figure 2, The diagram of a radial line for semi–infinite parallel conducting plane structure and the corresponding NTL model.

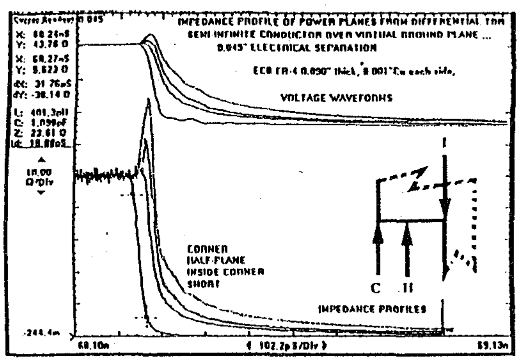


Figure 3, The measured time domain reflection voltage waveforms together with the extracted nonuniform impedance profiles for three cases: right angle sector, a half plane and 270^0 sector. (h=90mil, material:FR–4)

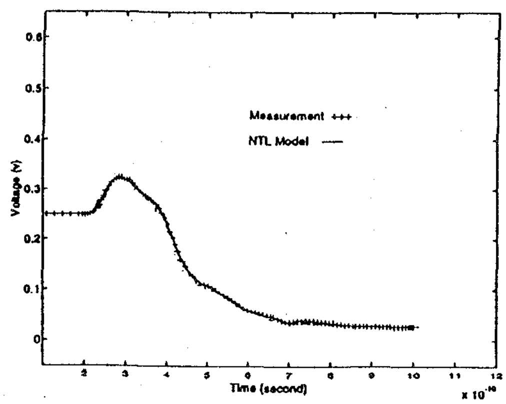


Figure 4, The measured TDR response and the simulated data for a measurement based NTL model for a MLC package.

Now, the input impedance of power/ground plane structures can be obtained by truncating the measured nonuniform impedance profile and evaluating the input impedance at a given frequency by using the piecewise impedance model. For the case of a typical parallel power/ ground plane structure in a MLC package, the measurement based NTL model is validated by comparing the simulation data with the measured response shown in Figure 4, the calculated input impedance for the NTL model is alo shown in Figure 5.

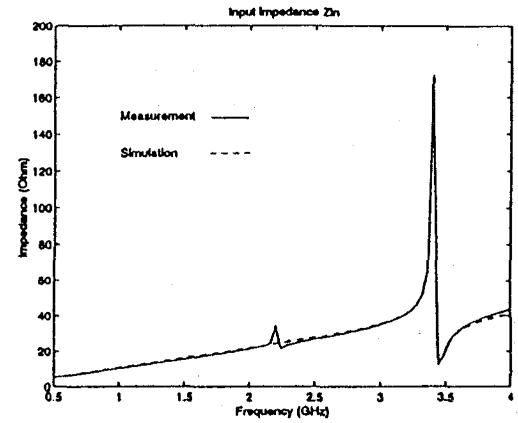
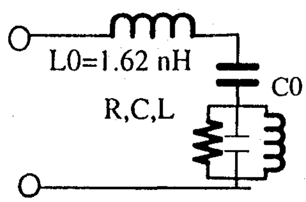


Figure 5, The input impedance of the measured nonuniform impedance profile in Figure 4.

An alternative equivalent circuit model shown in Figure 6 consisting of R,L,C lumped elements is proposed to simulate the switching noise and ground bounce with the associated package resonance. The circuit parameters of the model are obtained by deriving a lumped element network having the same input impedance as the measured nonuniform transmission line model over a desired frequency range. As an example, Figure 5 shows the input impedance valid through 4 GHz including the first resonance corresponding to the structure. The equivalent circuit elements L0 (the low frequency effective inductance) and C0 (stray capacitance of parallel planes) are readily calculated from the impedance profiles by using the techniques given in references [6,7] and {R, L, C} are determined by minimizing the error function representing the difference between the measured input impedance and the values of the input impedance for the model evaluated over the given frequencies in a least–square sense . The minimization of the error function was performed by utilizing the conjugate gradient algorithm in an iterative manner [8–10]. The simulated result for the input impedance of the lumped model is compared with the measured input impedance in Figure 5 and the good agreement validates the accuracy of the model through 4 GHz. Note that the power/ground plane resonance at higher frequencies has also been calculated by rigorous electromagnetic simulation such as the FDTD method as reported in [4].



$R = 107\Omega, L = 0.04nH, C = 52.9pF$

Figure 6, Lumped element model of the power/ground plane structure.

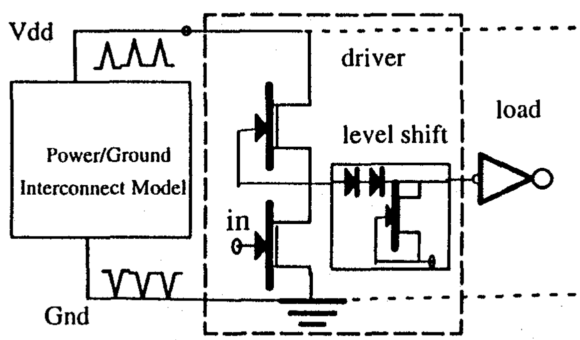


Figure 7, The circuit diagram of the GaAs FL.

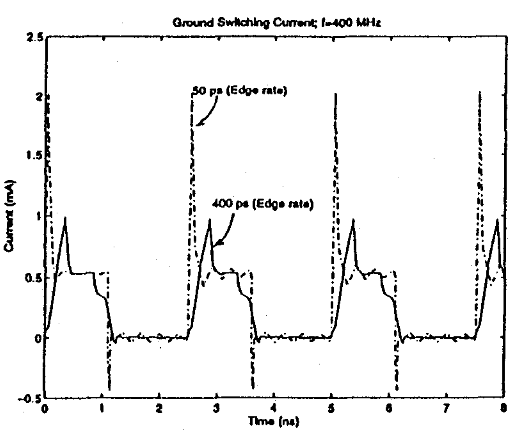


Figure 8, Switching currents vs edge rates for a GaAs FL inverter with 400 MHz clock rate.

SWITCHING NOISE SIMULATION

As an example, the circuit diagram of the GaAs FL inverter with the associated power/ground interconnect structure shown in Figure 7 is used as a vehicle to investigate the effects of switching noise in circuit simulations. The waveshape of ground switching currents due to the input clock signal switching from one logic level to another vs edge rates of the input signal are shown in Figure 8. The resulting frequency harmonics of switching currents are used to determine the frequency band over which the power/ground structures should be modelled.

For a GaAs FL inverter having 400 MHz clock rate with 50 ps edge rate, the simulated result for switching noise including the power/ground plane model is shown in Figure 9 for two cases. In one case the complete equivalent circuit incorporating the resonance is considered whereas in the other case the first order model excluding the resonance is used. For the case of high frequency model, it is obvious that switching noise consists of two major components, one is spike noise due to the switching circuit operating in the underdamped mode and the other is resonant noise to account for the effect of package resonance. However, for the case of the low frequency model based on the first order approximation, only spike noise appears in the simulated result. As shown in Figure 10, the amplitude of resonant noise becomes negligible when the edge rate of the excited input signal is slower than 400ps for this typical GaAs FL inverter. In addition, the simulations of switching noise based on the high frequency model of power/ground systems are also examined for the GaAs FL inverter with 1GHz clock rate. The maximum amplitude of spike noise as a function of edge rates is shown in Figure 11. The result can be used to control the reduction of noise immunity due to switching noise during the early design phase.

In conclusion, accurate measurement based high frequency model for power/ground plane associated with typical multilayer packages is presented. The model is shown to be useful for the simulation of switching noise and ground bounce in high speed analog, digital and mixed signal integrated circuits.

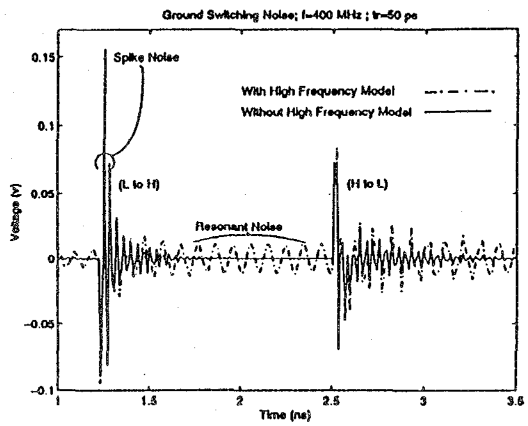


Figure 9, The simulated result of switching noise for a GaAs FL inverter

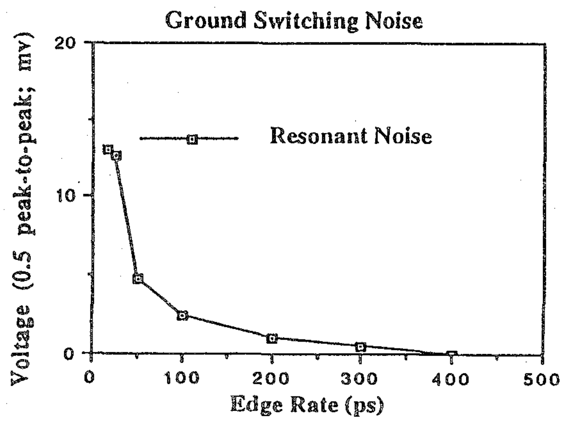


Figure 10, Resonant noise vs Edge rates.

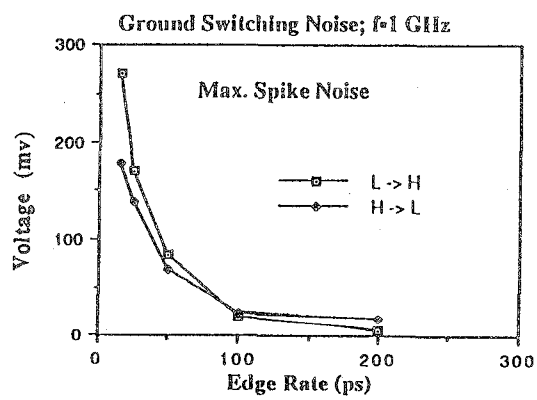


Figure 11, Spike noise vs Edge rates (f=1GHz).

ACKNOWLEDGEMENT

The contributions of Mr. Bo Janko for this work are gratefully acknowledged. This work was supported in part by Tektronix Inc. in Beaverton, Oregon.

REFERENCES

[1] A. R. Djordjevič and T. K. Sarkar, "An Investigation of Delta–I Noise on Integrated Circuits", *IEEE Trans. EMC*, pp. 134–147, May 1993

[2] R. Senthinathan and J. Prince, "Simultaneous Switching Ground Noise Calculations for CMOS Devices", *IEEE J. SSC*, pp. 1383–1388, Dec. 1993

[3] J. R. Phillips, M. Kamon and J. White, "A FFT–Based Approach to Including Non–ideal Ground Planes in A Fast 3–D Inductance Extraction Program", *IEEE CICC*, pp. 8.3.1–8.3.4, 1993

[4] R. Mittra, S. Chebolu and W. D. Becker, "Efficient Modeling of Power Planes in Computer Packages Using the FDTD Methods", *IEEE Trans. MTT*, pp. 1791–1795, Sept. 1994

[5] J. M Jong, B. Janko and V. K. Tripathi, "A Model of Semi–infinite Parallel Couducting Planes", *IEEE EPEP*, pp. 211–213, Oct. 1993

[6] J. M Jong and V. K. Tripathi, "Time Domain Characterization of Interconnect Discontinuities in High Speed Circuits", *IEEE Trans. CHMT*, pp. 497–504, August 1992

[7] J. M. Jong, B. Janko and V. K. Tripathi, "Equivalent Circuit Modeling of Interconnects from Time Domain Measurements" *IEEE Trans. CHMT*, pp. 119–126, Feb. 1993

[8] V. K. Tripathi and A. Hill, "Equivalent Circuit Modeling of Losses and Dispersion in Single and Coupled Lines for Microwave and Millimeter–wave Integrated Circuits", *IEEE Trans. MTT*, pp. 256–262, Feb. 1988

[9] W. H. Press, S. A. Teukolsky, W. T. Vetterling and B. P. Flannery, *Numerical Recipes*, Cambridge University Press, 1992

[10] *Libra and Touchstobe Manul: Performance & Optimization*, Eesof Inc., 1989